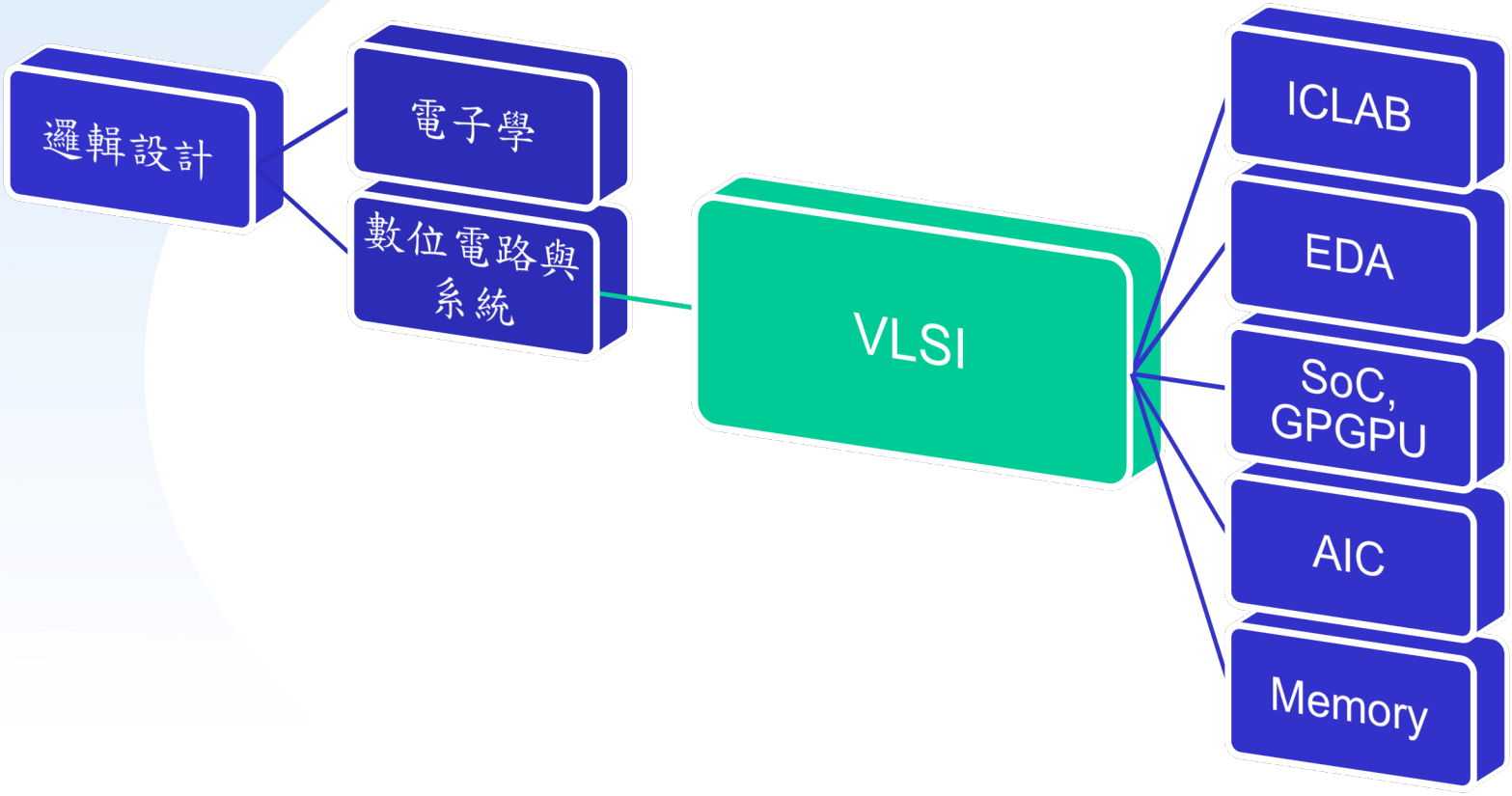
LAB Introduction

Road Map



LAB Schedule

- **Course website**
  - http://www.si2lab.org/course/vlsi2018/
  - Course discussion forum
  - telnet://kulu.twbbs.org
    Class -> 01_EE/ -> EE_Course/ -> EE_vlsi
- **TA:**
  - 呂蘊文、張育銘、曾駿哲 (ext.54238; ED430)

LAB Schedule

- ✓ **Individual study**
- ✓ **Lab room: ED220 or ED415**
  - CMOS Process Node (CIC Virtual Mixed-Mode 0.18um)
  - NDA signature, honor code required
- ✓ **Demo Schedule**
  - TBD
- ✓ **Grading**
  - 2 projects (30%)
  - 4 Exercise ( )

TA Course Schedule

- ✓ Lec01: Introduction to Hspice
- ✓ Lec02: Schematic and Layout Design
- ✓ Lec03: Verilog Gate Level Design
- ✓ Lec04: Midterm Project
- ✓ Lec05: Post Simulation
- ✓ Lec06: Final Project