An eCrystal Oscillator with Self-Calibration Capability

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Abstract—This paper reports an embedded crystal (eCrystal) oscillator which is capable of compensating process, voltage, and temperature (PVT) variation. The delay behaviors of two different delay cells are exploited for the delay estimation. Then the estimated delay is parameterized by a second order approximated function. According to the estimated delay, the eCrystal oscillator is able to calibrate the frequency error without any external reference. A 40MHz oscillator is implemented in a 90-nm CMOS technology with area of 0.4mm² by an all-digital approach. The fabricated chip is measured under supply voltage from 0.9V to 1.1V and temperature range from 0°C to 75°C with active power consumption of 237μW.

I. INTRODUCTION

With CMOS process shrinking toward deep submicron (DSM) scale, the functionality of a chip covers a variety of applications. The highly integrated system-on-a-chip (SoC) devices have the advantages of increased system performance and reduced system power consumption. However, the oscillation clock source is conventionally based on a quartz crystal oscillator which is incompatible to the CMOS process. The incompatibility in the process results in extra cost and volume in the board-level integration and, hence, large power is wasted from the external oscillator. For the purpose of reducing system volume and power, the on-chip oscillator becomes necessary.

The key challenge to an on-chip oscillator design is to maintain the stability of frequency due to process, voltage, and temperature (PVT) variations. The bandgap regulator techniques [1], [2] are applied for suppressing the supply voltage variation. The process and temperature variations are either sensed or compensated by carefully refining the transistor configurations. The current limiting technique [3] is proposed to compensate temperature variation. Nevertheless, these methods are not easily portable when fabrication process migrates toward DSM scale. Moreover, there exists a design barrier when the conventional bandgap regulator operates under 1.2-V supply voltage [4]. In contrast, the all-digital design approach is power efficient, portable with process migrations, and easy to be adopted in low supply voltage.

Fig. 1. Delay spread of a delay line composed of 100 buffers connected in a series under PVT variations.

This paper proposes an embedded crystal (eCrystal) which is capable of calibrating PVT variations in an all-digital approach. In the following section, the proposed eCrystal system architecture is introduced. The detailed blocks are explained in Section III. Section IV shows the chip implementation and the measurement result. Finally, in Section V, the eCrystal oscillator is concluded.

II. SYSTEM ARCHITECTURE

In the CMOS process, gate delay is strongly affected by PVT variations and can be modeled as a function of PVT, that is, $D(P, V, T)$. Fig. 1 shows the delay spread of a delay line composed of 100 buffers connected in a series in a 90-nm CMOS process. The delay varies widely from 2.8ns to 7.5ns with different supply voltage and temperature across process corners of SLOW, TYPICAL, and FAST which are provided by a foundry. If the delay line is applied in a free running ring oscillator, PVT variations make the oscillation frequency unstable. Even if the process variation is calibrated in a post-process testing, the frequency variation is still high and unpredictable due to the unknown supply voltage and operation temperature. Therefore, we propose a unified approach to estimate the present gate delay in a view of a relative delay behavior regardless of the individual effect from

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Fig. 2. Relation between the delay of the reference delay cell to the delay ratio.

Fig. 3. System architecture of the eCrystal oscillator.

PVT variations. Define the delay ratio $R(P,V,T)$, which is a function of PVT conditions,

$$R(P,V,T) = \frac{D_{comp}(P,V,T)}{D_{ref}(P,V,T)} \quad (1)$$

where $D_{comp}(P,V,T)$ and $D_{ref}(P,V,T)$ are delays of the compared delay cell and the reference delay cell respectively in the present PVT condition. The delay ratio of these two delay cells is aimed to estimate the delay of the reference delay cell. To strengthen the difference of the delay behavior to PVT conditions in these two delay cells, we adopt NAND gate as the compared delay cell and BUFFER gate as the reference delay cell. Sweeping the PVT conditions of three process corners each with voltage range from 0.9V to 1.1V and temperature range from 0°C to 75°C, the delay of the reference delay cell to the delay ratio is plotted in Fig. 2. The curve of the reference delay can be approximated by $\tilde{D}_{ref}(P,V,T)$, which is a second order function of the delay ratio $R(P,V,T)$, that is

$$\tilde{D}_{ref}(P,V,T) = aR^2(P,V,T) + bR(P,V,T) + c \quad (2)$$

where a , b , and c are process dependent parameters (PDPs). Three process corners are fitted by three sets of PDPs. The PDPs can be obtained by a post-process testing with at least three voltage and temperature conditions in the curve.

From the above formulation, we propose a system architecture for the eCrystal oscillator as shown in Fig. 3. The delay ratio estimator first estimates the delay ratio of two

Fig. 4. Circuit of the delay ratio estimator.

different delay cells. With the estimated delay ratio, denoted as $\tilde{R}(P,V,T)$, and the obtained PDPs, the mapper is able to have the delay of the reference delay cell, denoted as $\hat{D}_{ref}(P,V,T)$. Based on the obtained delay information, the control code, C , is calculated for the digitally controlled oscillator (DCO) to generate the desired frequency.

III. CIRCUIT DESIGN

A. Delay Ratio Estimator

In the delay ratio estimator, the delay ratio of two delay cells is going to be examined. Setting a compared delay line and a reference delay line, we denote the number of delay cells in the compared delay line as N_{comp} and the number of delay cells in the reference delay line as N_{ref} . The two delay lines are connected to a phase detector, and $LEAD$ is the decision output of the phase detector. Feeding a step function input to these two delay lines at the same time, we can examine the delay ratio. If the propagated signal through the compared delay line is faster than the reference delay line, $LEAD$ will be 1. Therefore, we can tell the delay ratio from

$$LEAD = \begin{cases} 1 & \text{if } R(P,V,T) < \frac{N_{ref}}{N_{comp}} \\ 0 & \text{if } R(P,V,T) \geq \frac{N_{ref}}{N_{comp}} \end{cases} \quad (3)$$

Accordingly, we can design the number of delay cells in such a comparison pair for examining the delay ratio. As shown in Fig. 4, a series of comparison pairs are set with the same number of delay cells in the reference delay lines and increasing number of delay cells in the compared delay lines. Let $LEAD[i]$, i from 0 to $N-1$, denote the N output signals of the phase detectors. $LEAD[i] = 1$ indicates the delay ratio $R(P,V,T) < N_{ref} / N_{comp,i}$ where $N_{comp,i}$ is the number of delay cells in the compared delay line in the i th comparison pair and N_{ref} is the number of delay cells in the reference delay line. Due to the increasing delay cells in the compared delay lines in the comparison pairs, $LEAD[i]$ will be presented as a series of 1 followed by a series of 0. If $LEAD[i] = 1$ for i from 0 to k

Fig. 5. Circuit of the digitally controlled oscillator.

and $LEAD[i] = 0$ for i from $k+1$ to $N-1$, the delay ratio $R(P, V, T)$ is bounded in

$$\frac{N_{ref}}{N_{comp,k+1}} \leq R(P, V, T) < \frac{N_{ref}}{N_{comp,k}}. \quad (4)$$

Therefore, the estimated delay ratio $\tilde{R}(P, V, T)$ is estimated as the middle point of the above two boundaries, that is

$$\tilde{R}(P, V, T) = \frac{1}{2} \left(\frac{N_{ref}}{N_{comp,k+1}} + \frac{N_{ref}}{N_{comp,k}} \right). \quad (5)$$

We set up 49 comparison pairs to partition the estimated delay ratio into 50 intervals. The number of delay cells in the reference delay line is 420 in every comparison pair and the numbers of the delay cells in the compared delay lines are from 413 to 461. From the comparison result $LEAD[i]$ of the series phase detectors, the estimated delay ratio can be obtained according to the look-up table which records the delay ratio values in (5).

B. Mapper

Once the delay ratio is estimated, the control code can be calculated in this block. We take the estimated delay ratio $\tilde{R}(P, V, T)$ into (2). The estimated delay of the reference delay cell is

$$\hat{D}_{ref}(P, V, T) = a\tilde{R}^2(P, V, T) + b\tilde{R}(P, V, T) + c. \quad (6)$$

From (6), the delay of the reference delay cell is estimated. The DCO is based on a ring oscillator with adjustable delay cell length in the delay line. The desired frequency, f_{des} , is

$$\begin{aligned} f_{des} &= \frac{1}{2 \cdot D_{path}(P, V, T)} \\ &= \frac{1}{2 \cdot [\hat{C}\hat{D}_{ref}(P, V, T) + D_{extra}(P, V, T)]} \\ &\cong \frac{1}{2 \cdot [\hat{C}\hat{D}_{ref}(P, V, T) + D_{extra}]} \end{aligned} \quad (7)$$

where $D_{path}(P, V, T)$ is the total delay in the delay path, which is equal to the delay of the reference delay line plus some extra

combinational delay, $D_{extra}(P, V, T)$, in the delay path. The extra combinational delay is also a function of PVT conditions. However, the variation is far less than the main delay line in the delay path and can be neglected. The extra combinational delay is rewritten as a constant D_{extra} . From (7), the calibrated control code can be derived as

$$\begin{aligned} C &= \frac{\frac{1}{2 \cdot f_{des}} - D_{extra}}{\hat{D}_{ref}(P, V, T)} \\ &= \frac{\frac{1}{2 \cdot f_{des}} - D_{extra}}{a\tilde{R}^2(P, V, T) + b\tilde{R}(P, V, T) + c} \end{aligned} \quad (8)$$

C. Digitally Controlled Oscillator

The DCO of adjustable delay cell length is proposed as shown in Fig. 5. The control code, C , is provided to be the number of delay cells in a delay line. The delay line is composed of the reference delay cell where the gate delay is estimated in (6). To select the number of the reference delay cells in the delay line, a path selector is applied to enable one of the possible delay paths according to the control code, C . The number of reference delay cells in the delay path is

Fig. 6. Simulation result (a) The control code to the PVT condition. (b) The calibrated frequency.

Fig. 7. Layout of the eCrystal oscillator.

therefore adjusted to C . The corresponding frequency is generated according to (7).

IV. IMPLEMENTATION AND MEASUREMENT RESULT

An eCrystal oscillator is designed and implemented in a 90-nm CMOS process. The simulation environment includes process corners from SLOW to FAST, voltage range from 0.9V to 1.1V of step size 0.02V, and temperature swept from 0°C to 75°C in every 25°C. Setting the desired frequency as 40MHz, the simulation result is shown in Fig. 6. The control code is between 83 and 218 for the estimated delay from 150ps to 56ps. As a result, the frequency to the PVT variation is calibrated to around 40MHz.

Fig. 7 shows the chip layout, and the area of the eCrystal oscillator, including the delay ratio estimator, mapper, and DCO, is about 0.4mm². The floor plan is designed to separate the sensitive delay ratio estimator from the other circuits, whereas the mapper and DCO are combined with the other circuits. The chip is tested under voltage conditions from 0.9V to 1.1V stepped by 0.02V and temperature conditions from 0°C to 75°C in every 25°C. Total of the 44 conditions are tested, and the chip is able to calibrate the PVT variation. The measured output frequency is depicted in Fig. 8. The maximum frequency error is 3.5%. The whole chip consumes 971μW at 1-V voltage supply and 25°C condition when the eCrystal oscillator is operating at 40MHz. However, the total operation power of the eCrystal oscillator can not be obtained separately. If DCO is disabled by the RESET signal in Fig. 5 and the other signals of the eCrystal oscillator are kept steady, the measured power is 734μW. Therefore, we can reasonably derive the dynamic power of the eCrystal oscillator is 237μW. Finally, the comparison with other on-chip oscillators is listed in Table I. Comparing to [1], the proposed eCrystal oscillator is with less area and an order of power reduction. The frequency error is less than [2] and [3] whose frequency errors are 5% and 5.8% respectively. For comparing the overall performance, the power-frequency-error product (PFEP) is defined as a performance index, and the PFEP should be as small as possible. Except for [3], where the voltage is fixed at 1.2V, the proposed eCrystal oscillator has the best PFEP among the PVT variation tolerable designs.

V. CONCLUSION

An eCrystal oscillator is proposed as the on-chip oscillator. The present gate delay can be obtained by the relation between two delay cells that have different delay behaviors to PVT variations. The estimated delay is modeled as a second order

Fig. 8. Measured output frequency of the eCrystal oscillator.

TABLE I. ON-CHIP OSCILLATOR COMPARISON

Design	Proposed eCrystal oscillator	[1]	[2]	[3]
Technology	90 nm CMOS	0.25 μm CMOS	0.5 μm CMOS	0.13 μm CMOS
Target Frequency	40 MHz	7 MHz	12.8 MHz	10 MHz
Area	0.4 mm ²	1.6 mm ²	0.185 mm ²	160 μm ²
Power	237 μW*	1500 μW	400 μW	30 μW
Frequency Error	3.5 %	2.6 %	5 %	5.8 %
PFEP	829.5	3900	2000	174
PVT Variation Tolerable	YES	YES	YES	Fixed 1.2V

* Dynamic power

function of the delay ratio of the compared delay cell to the reference delay cell. As a result, a 40MHz eCrystal oscillator is implemented in a 90-nm CMOS process. The eCrystal oscillator can estimate the present delay due to PVT variations and generate the desired frequency in an all-digital approach which is power efficient and easily portable. The operating dynamic power is 237μW and the measured frequency error is 3.5% across voltage range from 0.9V to 1.1V and temperature range from 0°C to 75°C. The eCrystal oscillator can be integrated into SoC devices to generate a stable clock frequency without any external reference.

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