A Low Power All-Digital Signal Component Separator for Uneven Multi-Level LINC Systems

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Abstract— This paper presents an all-digital signal component separator (SCS) with low power overhead for uneven multi-level LINC (UMLINC) systems, including a multi-level phase calculator (MLPC) and a digitally-control phase shifter (DCPS) pair. The optimal gain level with branch mismatch consideration is proposed to achieve maximal average efficiency 44.82%. This SCS chip is manufactured in 90 nm standard CMOS process with an active area 0.5 mm². The required phases of branch signals and PA gain controls can be calculated by the proposed MLPC. Instead of four DACs, the DCPS pair with a continuous PVT monitor is also proposed to generate the phase-modulated signals accurately at IF frequency 80 MHz with 8-bit resolution. By applying voltage scaling and source gating on DSP functions and DCPSs respectively, 81.32% power cost of SCS can be reduced, and the overall power is only 0.65 mW. With the proposed SCS, the EVM of -31.06 dB using 64-QAM OFDM signals can be achieved for high-efficiency UMLINC systems.

I. INTRODUCTION

Recently, orthogonal frequency division multiplexing (OFDM) has been considered as a promising candidate for high data rate transmission in a mobile environment. One of the serious drawback is the high peak-to-average power ratio (PAPR) of OFDM signals, resulting in poor efficiency of linear power amplifier (PA). Linear amplification by nonlinear components (LINC) [1] has been proposed to maintain the PA efficiency along with good linearity, but the overall efficiency is still degraded by the isolated combiner as the outphasing angle difference between two branches increases. Nonisolated combiners have been proposed to improve the combining efficiency, but the linearity is sacrificed [2]. Accordingly, uneven multi-level LINC (UMLINC) [3] have been suggested to improve the combining efficiency by reducing the possibility of large outphasing angles. To apply these techniques, the PA implementations with two gain modes have been proposed [4], [5]. However, a low power SCS design to separate signal into two constant-envelope signals and give corresponding gain mode controls is still required for these high-efficiency systems.

To achieve an accurate separation with low power overhead, the SCS design is a design challenge. To achieve high separation accuracy, digital implementation [6] is assumed to be the best choice. Unfortunately, digital SCS requires four DACs, and the power of both DACs and DSP suffers from high operation speed due to the nonlinear separation process. Several

analog designs are proposed to reduce the power cost [7], [8], but it is difficult to realize nonlinear mathematical functions. Besides, those published chips still cost tens-milli-order power consumption, a significant overhead for the transmitter. A sub-mW SCS is proposed in our previous work [9]. However, the state-of-the-art solutions only consider conventional LINC and can be applied to UMLINC systems.

Accordingly, this work presents an all-digital SCS for UMLINC with minimal power overhead. First, this work discusses the limitation of PA gain levels with branch mismatch issues and finds the optimal level for maximal efficiency. For the SCS implementation, a multi-level phase calculator (MLPC) is included to calculate specified phases with corresponding PA gain mode controls. To reduce the power of high-speed calculations, the DSP functions can be operated at 0.5V to save power dissipation. Instead of four DACs, a power-of-two based digitally-control phase shifter (DCPS) pair with a continuous PVT monitor is proposed to generate the phase-modulated signals accurately. A source gating scheme is applied in DCPS to reduce the power overhead without sacrificing its linearity. Besides, this SCS also provides mismatch compensation capability to enhance the system performance.

This paper is organized as follows. In section II, the system behavior is introduced. Then the chip implementation details are described in section III. Section IV shows the system evolution results, followed by the conclusion in section V.

II. SYSTEM OVERVIEW

A. UMLINC Principle

Denote the baseband signal as $S_b(t) = S_i(t) + jS_q(t)$, then the transmitted signal $S(t)$ can be generally expressed as

$$S(t) = \text{Re} \{ (S_i(t) + jS_q(t))e^{jw_c t} \} = A(t) \cos(w_c t + \theta(t))$$

where $A(t)$ and $\theta(t)$ are the envelope and phase given by

$$\begin{aligned} A(t) &= \sqrt{S_i^2(t) + S_q^2(t)}, \\ \theta(t) &= \tan^{-1} \left(\frac{S_q(t)}{S_i(t)} \right). \end{aligned} \quad (1)$$

As shown in Fig. 1 (a), the concept of UMLINC is to separate the original signal $S(t)$ into two phase-only-modulated signals $S_1(t)$ and $S_2(t)$ with minimal outphasing angles to achieve maximal efficiency [3]. This work assumed that the high efficiency PAs can provide two gain modes - high gain V_{HT} and low gain $V_{LT} = \beta V_{HT}$. Denote $S_1(t)$ and $S_2(t)$ as

$$\begin{aligned} S_1(t) &= \cos(w_c t + \theta(t) + \phi_1(t)), \\ S_2(t) &= \cos(w_c t + \theta(t) - \phi_2(t)), \end{aligned} \quad (2)$$

Fig. 1. (a) UMLINC schematic (b) Vector representation of different regions.

where the outphasing angles $\phi_1(t)$ and $\phi_2(t)$ can be derived:

$$\begin{aligned}\phi_1(t) &= \cos^{-1}\left(\frac{V_1^2(t) + 4A^2(t) - V_2^2(t)}{4V_1(t)A(t)}\right), \\ \phi_2(t) &= \cos^{-1}\left(\frac{V_2^2(t) + 4A^2(t) - V_1^2(t)}{4V_2(t)A(t)}\right).\end{aligned}\quad (3)$$

$V_1(t)$ and $V_2(t)$ representing PA gains are V_{LT} or V_{HT} decided by the envelope regions as shown in Fig. 1 (b). Since $S_1(t)$ and $S_2(t)$ only contain phase information, they can be generated by two phase modulators (PMs) directly with the calculated phases $\theta(t) + \phi_1(t)$ and $\theta(t) - \phi_2(t)$.

B. Branch Mismatch Issue and Optimal Level Decision

The branch mismatch degrades the linearity significantly, and this issue is more complex in UMLINC since the mismatches are different during gain mode switch. Since V_{HT} and V_{LT} reflect the gain of PAs, the gain mismatches between two branches or two gain modes will affect the separation correctness. Use the upper branch with high gain mode as the basis, the gain mismatches of the other cases are denoted as κ_{L1} , κ_{H2} , and κ_{L2} , then the exact gains are $V_{H1} = V_{HT}$, $V_{L1} = \kappa_{L1}V_{LT}$, $V_{H2} = \kappa_{H2}V_{HT}$, and $V_{L2} = \kappa_{L2}V_{LT}$. Therefore, $V_1(t)$ and $V_2(t)$ in (3) should be specified to these calibrated gain values, such that the gain mismatch can be considered during the signal separation [9]. Similarly, the phase mismatch can be compensated by adding corresponding phase offsets in different gain modes. Another consideration is the region cover range, the boundaries V_{LT} and V_{MT} should also be adjusted to ensure the correct cover range. Therefore, this work proposed a modified region boundaries as

$$\begin{aligned}\hat{V}_{LT} &= \frac{V_{L1} + V_{L2}}{2}, \\ \hat{V}_{MT} &= \frac{V_{H1} + V_{H2}}{2}.\end{aligned}\quad (4)$$

To achieve maximum efficiency, the gain ratio β decision is important, but the region cover range should also be considered to avoid signal distortion. A limitation is the minimal magnitude of Region 2 - $(V_{HT} - V_{LT})/2$ should be smaller or equal to the maximal magnitude of Region 1 - V_{LT} , then we can conclude the gain ratio should be larger than 1/3. Using 64-QAM 64-point OFDM signal as the signal source, Fig. 2 (a) shows the average combining efficiency

Fig. 2. (a) Optimal ratio of UMLINC (b) Efficiency comparisons.

with different gain ratio, and the optimal gain ratio is 1/3. To avoid the cover range violation caused by the gain mismatch κ_{L1} and κ_{L2} , the gain ratio is specified to 0.42 in this work (2.01 dB gain mismatch tolerance), corresponding to maximum 44.82% average efficiency. Fig. 2 (b) shows the average combining efficiency comparison between LINC and UMLINC, the average combining efficiency can be modified from 13.08% to 44.82%, resulting in 3.44x improvement.

III. CHIP IMPLEMENTATION

Figure 3 presents the chip block diagram and signal paths. The source signal from the baseband modem with 5 MHz bandwidth is 8x interpolated by an interpolation filter (linear phase 81-tap Kaiser FIR filter) first to extend the operation bandwidth for nonlinear calculation. Then the MLPC operating at 40 MHz calculates the 8-bit phase codeword and gain mode controls for PMs and PAs respectively. The mapper transfers the phase codewords to control codewords for the DCPS pair, which is behaved as PMs in this work, then the desired phase-modulated signals can be generated at IF frequency 80 MHz. The gain and phase mismatch values of different PA gain modes can be programmed in the registers by the serial peripheral interface (SPI), and the proposed SCS can balance the mismatch during the transmission.

To achieve low power and accurate SCS, this chip is partitioned into two independent power domains with different supply voltages. The default domain uses 1.0 V to interface with IO pads, and the DCPS pair also uses 1.0 V to achieve accurate results. The high-speed DSP, including the interpolation filter, MLPC, and the mapper are operated with 0.5 V supply voltage to reduce the power cost. To apply the voltage scaling with the standard-cell-based design procedure, the cell behavior and timing information under 0.5 V supply voltage are simulated and re-calibrated, then the cell library after picking out the cells which can work normally is reconstructed. With the reconstructed cell library, the DCP functions can be implemented by exploiting standard-cell-based design procedure.

A. MLPC Design

Figure 4 is the detail block diagram of MLPC. The major work of MLPC is to calculate $\theta(t)$, $\phi_1(t)$, $\phi_2(t)$, and the gain-mode controls for PAs according to the input signal magnitude dynamically. Before the calculation of outphasing angles $\phi_1(t)$ and $\phi_2(t)$, the level values and region boundaries

Fig. 3. Chip block diagram with power domain partitions.

Fig. 4. MLPC block diagram.

considering gain mismatch are calculated in the boundary calculation first. Then the level decision decides the gain-mode of PA depending on the region of input signal magnitude. Besides, it also outputs the corresponding $V_1(t)$ and $V_2(t)$ for the phi values calculation, which is the most complex operation in MLPC. Due to the increased propagation delay by voltage scaling, the critical delay becomes a design challenge, especially the long-bit division. To reduce the critical delay, three pipelines are inserted into the division to meet the timing requirements. The arc-cosine function is implemented by a look-up-table (LUT) to reduce the complexity. Similarly, the theta calculation in (1) is also implemented by the same way.

B. Low Power DCPS Pair with Continuous PVT Monitor

Figure 5 shows the proposed DCPS architecture consisting of two-stage delay-lines with 10-bit coarse-tune codeword C and 4-bit fine-tune codeword F to achieve adequate delay range and accuracy. The delay-line is based on power-of-two architecture to avoid complex codeword encoder, and a source gating is proposed to reduce the power waste. An “AND” cell is added before the delay cells in each coarse-tune sub-stage to avoid extra operation when the sub-stage delay is unused. The “AND” gate on the non-delay path is also necessary to keep power-of-two delay property and eliminate the loading difference between two paths. The fine-tune stage can achieve ps-level resolution by tuning the loading from gate capacitance. Besides, the DCPS pair can also provide a specified phase offset ϕ_c to eliminate the phase imbalance according to the gain modes from MLPC.

The mapper transfers the 8-bit phase codeword P to 14-bit $\{C, F\}$ by following equations:

$$C = \left\lfloor \frac{C^{(M)}P}{256} \right\rfloor, F = \left\lfloor \left(\frac{C^{(M)}P}{256} - \left\lfloor \frac{C^{(M)}P}{256} \right\rfloor \right) \lambda + \frac{F^{(M)}P}{256} \right\rfloor, \quad (5)$$

where $\{C^{(M)}, F^{(M)}\}$ is the code set corresponding to one

Fig. 5. DCPS based on power-of-two architecture.

Fig. 6. (a) PVT monitor block diagram (b) Tracking behavior.

IF clock period, and λ is the resolution ratio of two stages. $\{C^{(M)}, F^{(M)}\}$ and λ are varying with PVT, so a continuous monitor is required to ensure the accuracy. Fig. 6 (a) shows the proposed PVT monitor block diagram. Two delay-lines are duplicated for continuous monitoring without affecting the normal SCS operations, and a phase detector (PD) is added to construct a delay-lock-loop (DLL). By giving specified codewords $\{C_3, F_3\}$ and $\{C_4, F_4\}$ as shown in Fig. 6 (b), the required parameters can be detected continuously by repeating the tracking states. Each repeated tracking costs 5 to 25 cycles to converge depending on PVT varying amount. Observing the coarse-tune control codewords of DCPS4 are always small, so the power overhead is low since most coarse-tune delay sub-stages are not used and can be gated.

IV. EXPERIMENTAL RESULTS

The proposed SCS chip is fabricated in 90 nm 1P9M standard CMOS process. Table I shows the DCPS measurement results under different supply voltages, and the output delay can cover our target period 12.5 ns. The minimum resolution 13.86 ps can be achieved typically, which also implies 0.4° phase compensation can be achieved. Although the DCPS performance is affected by operation environments, the continuous PVT monitor can detect the correct $C^{(M)}, F^{(M)}$, and λ accurately for the codeword mapper with low power overhead 140 μ W. Therefore, Fig. 7 (a) shows the measured DCPS output delay with different phase codewords, providing 8-bit resolution with root-mean-square (RMS) error 11.57 ps (0.33°). Fig. 7 (b) presents the power consumption of a DCPS operating at 80 MHz. Smaller codeword costs less power due

TABLE I
DCPS MEASUREMENT RESULTS

Supply Voltage	0.9 V	1.0 V	1.1 V
Max. Coarse-tune Delay	48.98 ns	40.75 ns	36.11 ns
Coarse-tune Resolution	48.20 ps	40.89 ps	36.71 ps
Max. Fine-tune Delay	0.25 ns	0.21 ns	0.19 ns
Fine-tune Resolution	16.43 ps	13.86 ps	12.43 ps

Fig. 7. (a) DCPS delay (b) DCPS power vs. Phase codeword.

Fig. 8. Verification platform.

Fig. 9. Output spectrum.

to the source gating scheme on the unused sub-stages. Since the phase codeword is near norm distribution during normal operation, the average power of a DCPS is $74 \mu\text{W}$ typically.

To verify the UMLINC system behavior with the proposed SCS, a verification platform is constructed as shown in Fig. 8. The pattern generator (Agilent 16902A) provides the 64-QAM 64-point OFDM baseband signal with 5 MHz bandwidth and 8-bit quantization for the SCS chip, and the branch mismatch values can be programed into the chip registers by SPI interface from a micro control unit (MSP430). The measured SCS output waveforms including the phase-modulated signals and gain controls are sampled and stored in the oscilloscope (LeCroy 4000A), which provides maximum 20 GHz sampling resolution. Then these data are feedback to a front-end behavior model (including the filters, dual-gain PA with branch mismatch) to evaluate the system performance. Fig. IV shows the output spectrum with 1 dB gain and 10° phase mismatches. By using the proposed SCS with the mismatch compensation, the out-of-band radiation can be reduced, and the system error vector magnitude (EVM) of -31.06 dB is achieved.

The power of DSP blocks with 40 MHz operation speed is reduced to $359 \mu\text{W}$ by scaling the supply voltage to 0.5 V, resulting in 74.17% power reduction. The chip summary and comparisons are shown in Table II. Only this work presents the SCS implementation for UMLINC systems to further enhance the amplification efficiency. This work also extends the mismatch compensation in [9] to UMLINC for linearity improvement. Although this work integrates more functions and achieves better performance, the power is still smaller than [9] due to modified circuit designs. By using source gating and voltage scaling for the DCPSs and DSP blocks respectively, 81.32% power can be reduced as shown in Fig. 11. The overall SCS chip consumes only $647 \mu\text{W}$, a significant improvement comparing to state-of-the-art SCS designs.

Fig. 10. Chip photograph.

Fig. 11. Power reduction schemes.

TABLE II
CHIP SUMMARY AND COMPARISONS

	[7]	[8]	[9]	This work
Technology	0.35um CMOS	0.25um CMOS	90nm CMOS	90nm CMOS
Design Strategy	Analog	Analog	Digital	Digital
Supply Voltage	5.0V	2.5V	1.0V/0.5V	1.0V/0.5V
Operation Frequency	100MHz IF	20MHz Baseband	100MHz IF/ 50MHz DSP	80MHz IF/ 40MHz DSP
Active Power	80mW	45mW	0.95mW	0.65mW
Signal Source	DQPSK	64QAM	64QAM	64QAM
	OQPSK	OFDM	OFDM	OFDM
EVM	N/A	-34dB	-29.81dB	-31.06dB
Mismatch Comp.	No	No	Yes	Yes
Target System	LINC	LINC	LINC	UMLINC

V. CONCLUSION

An all-digital SCS for UMLINC system is presented in this work. The optimal gain level and the separation process considering the branch mismatch are proposed. The required separation DSP functions are implemented, and the power can be reduced by voltage scaling. Besides, the phase-modulated signals can be generated by a low-power DCPS pair without DACs. Therefore, an accurate SCS with low power overhead is achieved for high-efficiency UMLINC systems.

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