A 2.37Gb/s 284.8mW Rate-Compatible (491,3,6) LDPC-CC Decoder

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Abstract

In this paper, a (491, 3, 6) time-varying LDPC-CC decoder chip supporting five code-rates is implemented in 90nm CMOS technology. The decoder containing 5 processors occupies 2.24mm^2 and provides twice faster decoding convergence speed. Maximum throughput 2.37Gb/s is measured under 1.2V supply with a 0.024nJ/bit/proc energy efficiency. Keywords: LDPC-CC, high throughput.

Introduction

Due to high demands on error-correcting performance and the decoding throughput, low-density parity-check block codes (LDPC-BCs) and LDPC convolutional codes (LDPC-CCs) draw great research interests. As compared with LDPC-BCs, LDPC-CCs possess many advantages including near Shannon limit performance, variable length of data frame, flexible code-rate through puncturing, simple encoding circuitry, as well as low routing complexity in the decoder architecture. However, LDPC-CCs rarely appear in system specification for its bottlenecks of the long decoding latency, high power consumption, and low-to-moderate decoding throughput. The maximum measured throughput in previous literatures was only 600Mb/s and difficult to compete with LDPC-BCs [1], [2].

Fig. 1 shows (14,3,6) LDPC-CC decoder architecture as an example, which is a serial concatenation of multiple processors. Each processor decoding a $(m_s + 2)$ length sliding widow on the trellis diagram can be taken as one iteration in LDPC-BCs. Every row in the processor behaves like FIFO and can be implemented by registers or memories. There are 4 issues to design a high performance LDPC-CC decoder: 1) More processors can obtain better decoding performance but extend longer latency and result in similar throughput; 2) High node-level parallelism, e.g. more check node units (CNU) and variable node units (VNU), can achieve higher throughput but cause enormous message bandwidth; 3) Register-based FIFO can support unlimited bandwidth but yield expensive power and area costs; 4) Memory-based FIFO can reduce power consumption but suffer severe memory conflict. To overcome these issues, the work combining algorithm level, node level optimization, and a hybrid-partitioned FIFO is presented to achieve over 2Gb/s throughput with competitive power consumption and chip area.

Proposed Algorithm and Architecture

Fig. 2 demonstrates the algorithm-level optimization to accelerate the decoding convergence speed by using the on-demand variable node activation (OVA) scheduling technique [3]. The main idea is to change the variable activation location leaving from the processor to the position right before each check node input. The OVA scheduling is similar to the layered decoding

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Fig. 1. The (14, 3, 6) LDPC-CC decoder and conventional processor architecture. Note that the constrain length $m_s=14$, VN degree $d_v=3$, CN degree $d_c=6$ in this example.

in LDPC-BCs that check nodes could access the most recent messages. The original VNU can be disassembled into several sub-VNU (SVNUs) and distributed within a processor. Since the equation of VN-to-CN messages (e.g. n_1 and n_2 in Fig. 2) has two common terms, we may calculate n_2 from n_1 by deducting m_2 (done by pre-SVNU) and adding m_1 (done by post-SVNU). Therefore, the channel values (i.e. u and v) are concealed in VN-to-CN messages and the storage space of channel values can be removed from processors to save 17% memory.

When the channel values are concealed within the summation values, the bit-width of each message should be adjusted to avoid truncation error. In the situation of w -bit channel value, the summation values needs $(w + 2)$ -bit. Since the operations of pre-SVNU and post-SVNU are independent, they can be re-timed such that the messages between them only need $(w + 1)$ -bits. The original critical path from CNU to post-SVNU is also diminished by one adder delay.

On-Demand Variable-Node Activation (OVA) Scheduling

Fig. 2. Algorithm level optimization (OVA scheduling with concealing channel values).

Fig. 3. BER performance of Log-BP algorithm (floating-point) and our proposed scheduling in Normalized Min-Sum algorithm with scaling factor 0.875 (fixed-point (6,2)) under AWGN channel.

Fig. 3 is the bit-error-rate (BER) performance of the rate-compatible (491, 3, 6) time-varying LDPC-CC proposed in [4] under AWGN channel. In contrast to log-BP algorithm with 10 processors, the proposed algorithm with 5 processors can achieve similar or even better performance in all code-rates. Therefore, only half number of processors are required under the same performance, leading to half decoding latency reduction as well.

In the original structure of Fig. 1, the LDPC-CC decoder can only decode one bit in one cycle, so the information throughput will be f_{clk} Mb/s at f_{clk} MHz clock frequency. To increase throughput, the node level optimization duplicates both CNUs and VNUs to ρ (folding factor) units and the decoder throughput becomes $(\rho \times f_{clk})$ Mb/s. The proposed folding technique primarily duplicates the combinational logic while the sequential circuits are only slightly increased. In the meantime, the FIFO structure are also modified accordingly to provide sufficient input data for operation units. Each FIFO in the conventional processor is segmented by ρ factor to support required bandwidth.

For irregular time-varying LDPC-CC with large folding factor, neither register-based FIFO with high power consumption nor memory-based FIFO with serious memory conflict is suitable. In order to making trade-off between bandwidth and power, the hybrid-partitioned FIFO structure is presented. The first step is calculating the length of the longest continuous sectors of every folded row. Then sectors are to be merged into one memory bank together, where the depth of the memory bank is the minimum value of the sector lengths. If the original sector is larger than the memory depth, the excess part is still stored in registers. This procedure continues to merge sectors until the memory depth is less than a pre-defined parameter. In this work, 50% of messages in each processor are partitioned into three two-port memories (10.5 Kbits) and the clock buffers are also reduced by 54%.

Implementation Results

Fabricated in 90nm 1P9M CMOS process, our test chip integrates the OVA scheduling with concealed channel values, folding architecture, re-timed SVNU, and hybrid-partitioned FIFOs. Key features and performance comparison are given in Table I. The decoder chip occupies $2.24mm^2$ area with 479K gates and 52.5Kb SRAM. Measurement results show that the decoder draws 284mW under 1.2V supply voltage while running

at 198MHz. Since the folding factor equals 12, the information throughput of the LDPC-CC decoder achieves 2.37 Gb/s. When supply voltage is scaled down to 0.8V as shown in Fig. 4, the power is reduced to 90.2mW with an energy efficiency of 0.0114nJ/bit/proc. Compared with other LDPC-CC decoders [1], [2], this work provides higher throughput, less area, and better energy efficiency. Compared with the Turbo decoder [5], this work achieves much higher throughput with lower power and less die area. In conclusion, our proposed LDPC-CC decoder outperforms state-of-the-art designs and has the potential to be one candidate for next-generation communication systems. The chip micrograph is shown in Fig. 5.

TABLE I
CHIP SUMMARY AND COMPARISON WITH STATE-OF-THE-ART

FEC Type	This work	[1]	[2]	[5]
LDPC-CC	LDPC-CC	LDPC-CC	LDPC-CC	Turbo Code
Constraint Length ^(a)	984	258	960	3200
Code-Rate	1/2, 2/3, 3/4, 4/5, 5/6	1/2	1/2	1/3
CMOS Technology	90-nm	90-nm	90-nm	0.13- μ m
Input Quantization	6 bits	8 bits	6 bits	-
Processor ^(a)	5	3	1	5.5
Memory	52.5 kb	-	23.04 kb	129 kb
Area (mm^2)	2.24	1.5	0.924	3.57
Frequency (MHz)	198 ^(b)	600	250	302
Data Rate (Gb/s)	2.37 ^(b)	0.6	2.0	0.39
Power (mW)	284 ^(b)	368.7	-	788.9
Energy Efficiency (nJ/bit/proc) ^(a)	0.024 ^(b)	0.2048	0.064	0.37
	Measured	Measured	Synthesis	Measured

^(a) these terms represent block size, iteration, and nJ/bit/iter in Turbo code

^(b) measured at BER=10⁻⁵ without early-termination at 1.2V supply for rate 1/2

Fig. 4. Measurement Results and the comparison with previous works.

Fig. 5. Chip micrograph.

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