A Novel Single-bit Input All Digital Synchronizer and Demodulator Baseband Processor for Fast Frequency Hopping System*

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ABSTRACT

A new synchronization circuit with only one-bit input for fast frequency hopping systems, which is being implemented, is proposed in this paper. To companion with the one-bit input synchronizer, a one-bit input demodulator was also designed to test the viability of using single-bit input as a complete baseband processor for fast frequency hopping systems. Not only is the baseband chip low cost, it also provides a simpler analog front end. With those characteristics, the system becomes a low-cost overall system. The performance of the chip in terms of BER and synchronization offset are also comparable with other designs.

1. INTRODUCTION

Wireless technology is moving into the PWAN (Personal Wireless Area Network) era, where personal devices are connected together through wireless network. This means that personal information is placed in air. To ensure personal privacy, we need wireless modems with better security. Fast frequency hopping modem provides the best security compared with other wireless modems. However, the design of fast frequency hopping system is difficult, tedious, and expensive.

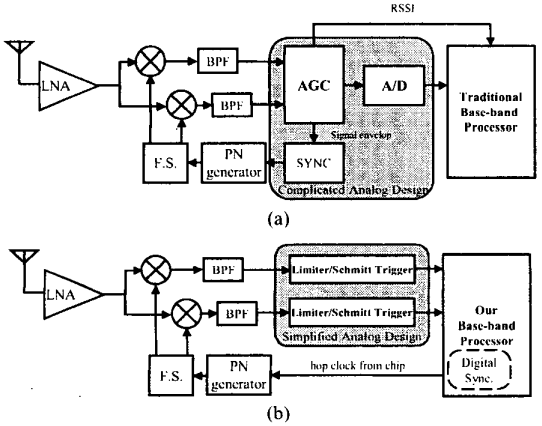

Figure 1. (a) AFE required by a traditional baseband processor; (b) simplified AFE for our baseband processor.

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The AFE (Analog Front End) of a traditional baseband design requires several complicated analog component as shown in Figure 1(a). Signal strength is also required for the traditional synchronization algorithms. Our new chip requires a simpler AFE design, as is shown in Figure 1(b). Most of all, a novel single-bit-all-digital synchronizer is used in our design. Therefore, with our new baseband processor, simpler AFE designs can be obtained.

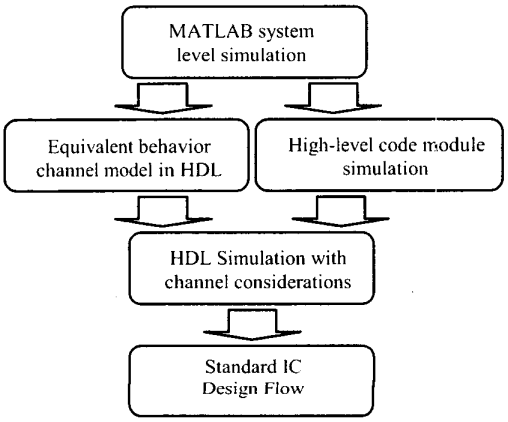

Figure 2. The design flow of our novel single bit input chip. High accuracy HDL channel models were designed to ensure correct hardware design at HDL level.

To verify this novel idea, we made several different simulations. The entire design process includes high level MATLAB simulation of the entire overall system. After confirmation of the behavior of the system, we used high-level code to simulate the algorithm of each individual module, such as the demodulator, ADPLL, etc. After several redesigns of the algorithm, we moved on to coding the modules into RTL code and then hardware implementation. Equivalent channel models were written in HDL code for HDL simulation to ensure the correctness of gate level simulation. The design process is shown in Figure 2.

Our design is easily scalable to different system specifications. However, for implementation, a specific system specification has to be defined. The specification of our system is shown in Table 1.

The rest of the paper is organized as follows: Section 2 briefly introduces several FH synchronization algorithms; Section 3

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describes the architecture and implementation issues of our chip; Section 4 compares the performance of our chip with various different previous designs; Section 5 is our conclusion.

Table 1. System Specification

Communication	FFH-SS
Channel Spacing	1 MHz
Hop Rate	1 MHz
Hopping Period	1 us
Hop Sequence	Not Required
Modulation	BFSK
Modulation Index	1 (orthogonal frequency)
Center Frequency Offset	10 MHz

2. SYNCHRONIZATION IN FH SYSTEMS

Hop clock synchronization is also called PN (Pseudo-Noise) code synchronization since the hop frequency is decided from the PN code. The process of PN code synchronization is done in two steps. The acquisition or initial synchronization phase locks the local hop sequence to be with in half the hop period of the received hopping sequence. Then, fine synchronization or tracking is used to find perfect synchronization.

2.1 Acquisition

There are two basic classes of acquisition circuit: the sequential search and parallel search scheme [1]. It is not efficient to implement the parallel scheme [2]. The sserial search method is more efficient. The idea of serial search is to search through all possible different phases and frequency of the PN code rate. There are several different search strategies presented in [2]. We used a rapidly synchronization acquisition system proposed in [8] for shorter acquisition time.

2.2 Tracking

The point of tracking is to reach perfect synchronization of the PN code. Besides, tracking loops has to compensate non-ideal effects such as Doppler effect, voltage swing, and temperature offset. Traditional tracking techniques include: (1) Time estimator method [4]; (2) Early-late gate tracking loop [6]; (3) Matched filter technique [7]. All required A/D and quite complicated hardware design.

In our chip, we used a time-integrator-based detector for signal-on-channel indication. This detector requires a single bit input of the channel information, and detects whether there is any signal on the channel. When the detector concludes that there is signal on the channel, it sends out a pulse, which indicates signal on channel.

3. ARCHITECTURE AND IMPLEMENTATION

3.1 Analog Front End

A traditional baseband design requires the AFE shown in figure 1(a). One of the most difficult circuits to design was the AGC (Automatic Gain Controllers) and the A/D converter. For FSK circuits, hard-limiters can be used to replace the more expensive AGC and A/D, which are more expensive in power and hardware complexity (Figure 1). Original synchronization techniques require energy of the received signal to detect whether the wanted signal is on the channel. Signal strength has to be extracted. This will require extra circuitry [5]. We used a single-bit all digital time-integrator-based detector to detect for signals in the channel. No extra circuitry is required for signal strength extraction. So the design is again made simpler.

3.2 Baseband Architecture

The entire architecture of our circuit is composed of a demodulator and a synchronizer. Both the synchronizer and the demodulator are single-bit input circuits. The synchronizer synchronizes the hop clock with only one-bit input signal. Then the synchronized clock information is sent to the demodulator. This is shown in Figure 3.

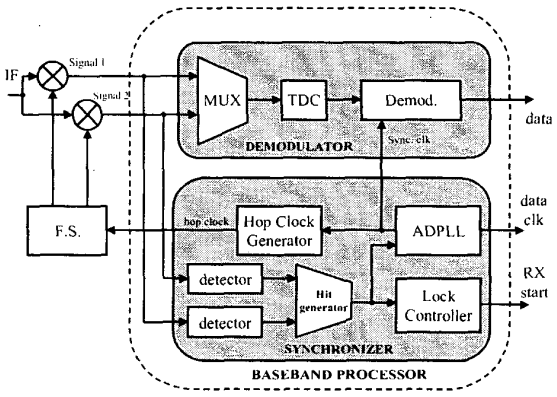

Figure 3. Overall architecture of the baseband processor

3.2.1 Demodulator

The demodulator is composed of a TDC (Time-to-Digital Converter) with up to 1GHz resolution and a demodulation circuit to demodulate the frequency information provided by the TDC, as is shown in Figure 3.

After the AFE down converted the received signal, the received signal will pass through a bandpass filter and several hard limiters. Only one bit of signal is provided to the TDC. The TDC retrieves the main frequency component of this signal. The demodulator then recovers the original data from the frequency component recovered by the TDC.

Our system assumes that the input signal is down converted to an offset baseband frequency. These parameters affect the lower acceptable bound of modulation index. The calculation on the relationship of TDC resolution and center frequency offset can be shown as follows:

$$\left\lfloor \frac{T_{upper} - T_{lower}}{T_{TDC}} \right\rfloor = \left\lfloor \frac{8hT_{period}}{T_{TDC}((\frac{T_{period}}{T_{center}}) - (4h)^2)} \right\rfloor > 2 \qquad (1)$$

where T_{upper} and T_{lower} are the upper and lower period of the input symbol with center frequency offset. T_{TDC} is the resolution of the TDC, T_{period} is the interval of the symbol, h is the modulation index.

3.2.2 Synchronization Circuit

The synchronization circuit is composed of time-integrator-based signal-on-channel detector, an ADPLL, and lock controller. The time-integrator detector detects whether there is any signal on the channel. A pulse is generated when the time-integrator detector indicates that there is any signal on the channel. Figure 3(c) shows how the time-integrator detector is connected to the ADPLL.

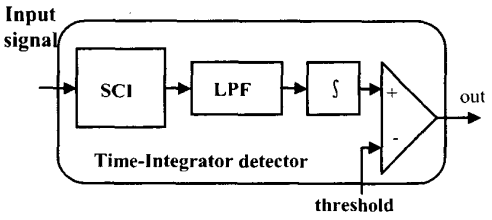

Figure 4. Structure of the time-integrator-based detector

The structure of the time-integrator detector is shown in Figure 4. The SCI (Signal-Change Indicator) senses for any changes in the signal. A LPF (Low Pass Filter) follows the SCI to combat two different effects: 1) there may not be a signal change for each observation; 2) even if there is signal change, there could have been some meta-stability issues due to the two clock domain. The integrator after the low pass filter is the time-integrator. The concept of time-integrator detector is to assume that the input signal strength is 1 when detector determines that there is any signal on the channel. Because the channel attenuates different frequencies with a different factor, the energy of the received signal for different hops are different. The detection without using the energy of the received signal is a good approximation.

4. SIMULATION AND PERFORMANCE

To ensure the performance of our chip, we made several performance evaluations on our chip. In Figure 5, the BER (Bit Error Rate) of our chip is compared with an ideal correlation demodulator.

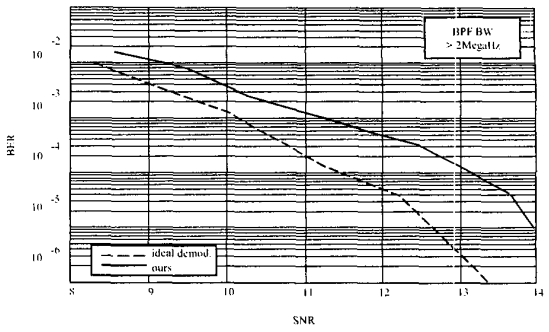

Figure 5. BER to SNR

The performance of the code tracking loop synchronizer was also simulated and compared with other designs, as is shown in Table 2. The result shows that our solution provides sufficient alignment of clocks for the demodulator to operate correctly. Besides, our precision is also higher than previous works.

Table 2. Comparison of synchronization precision for different designs

Design	Sync. precision	Technology
ours	95%	Single Chip Time-integrator & ADPLL
[6]	90%	Discrete Analog Early-Late Gate
[7]	86%	Discrete Digital Matched Filters

Table 3 shows the comparison of our chip area (in transistor count) and estimated chip power dissipation with other similar designs on demodulator and frequency hopping baseband processors. For comparison, we normalized area and power to data rate. The results are shown in Table 3. We can see that after normalization, our chip provides the smallest area and power consumption.

Table 3. Comparison of our chip with similar designs for FH systems. Area and power are normalized to data rate.

	ours	[9]	[10]	[11]
Data Rate	1Mbps	160Kbps	271Kbps	1Mbps
Area	19K	48K	11K	220K
Power Consumption	15mW	5.5mW	N.A.	105mW
Clock rate	32MHz	10MHz	100MHz	8MHz
Normalized area	19	300	40	220
Normalized power	15	34.37	N.A.	105

5. CONCLUSION

A novel single-bit input synchronizer and demodulator for fast frequency hopping systems was presented in this paper. The synchronizer uses a novel signal-on-channel indicator, based on time-integration concept. With the technologies introduced in this paper, future frequency hopping systems can be designed with lower cost (in designer time, power consumption, and hardware complexity) and with performance comparable to other designs. Current status of the chip is that it is being manufactured at TSMC, using 0.35um 1P4M technology.

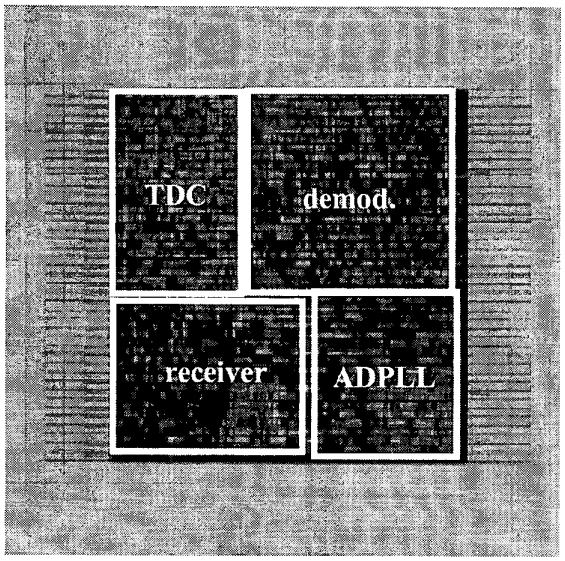

Figure 5. Layout View

Table 4. Chip Summary

Items	Specification
Technology	0.35um CMOS 1P4M
VLSI Type	Standard Cell
Function	FFH Synchronization & Demodulation Module
Chip Frequency	32MHz
Transistor	19K
Pin Count	32
Power Supply	+2.6V
Chip Size	2000um * 2000um
Power dissipation	20mW

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