14.6 A 1.8V 250mW COFDM Baseband Receiver for DVB-T/H Applications

Lei-Fone Chen, Yuan Chen, Lu-Chung Chien, Ying-Hao Ma, Chia-Hao Lee, Yu-Wei Lin, Chien-Ching Lin, Hsuan-Yu Liu, Terng-Yin Hsu, Chen-Yi Lee

National Chiao Tung University, Hsinchu, Taiwan

The DVB-T/H standard has been recently developed to provide video broadcasting services for hand-held devices [1]. The power consumption of a DVB-T/H baseband receiver must be strictly controlled in order to achieve long battery life. In response to this challenge a low-power COFDM baseband receiver for DVB-T/H is presented. It is comprised of an OFDM demodulator and forward-error correction (FEC) blocks for complete signal synchronization, mobile channel equalization, and data demodulation and correction. In addition, multi-stage power management (PM) is also exploited to eliminate redundant transition and power dissipation of baseband modules. With an area-efficient 2D equalizer (EQ), the proposed design can overcome 70Hz Doppler frequency (DF) resulted from 150km/h speed in the highest data rate mode, i.e. 31.67Mb/s. With single-port 158KBytes (158KB) embedded SRAM, it consumes only 250mW in the highest data rate mode specified in the DVB-T/H standards.

A block diagram of the design is shown in Fig. 14.6.1. It is comprised of an OFDM demodulator and FEC for synchronization, QAM-OFDM demodulation, Viterbi decoding, and RS decoding for standard 4.98Mb/s to 31.67Mb/s data rates. The OFDM designs with 36.56MHz work frequency are used to synchronize the symbol timing and carrier frequency offset (CFO) of the receiver, transfer the received signal from time to frequency domain, and then equalize the channel frequency response (CFR) of the mobile environment. A 2K/4K/8K-point FFT processor [2] is exploited to support the multiple symbol lengths of the DVB-T/H system. A 2D linear channel estimator (CE) is used to track the CFR variance caused by Doppler effects. The FEC subsystem, comprised mainly of the Viterbi decoder, Reed-Solomon (RS) decoder, and de-interleavers with 54.84MHz working frequency, is used for error correction. The path-merged Viterbi decoder [4] is used to reduce the trace-back complexity and save 40% Viterbi decoder power (40% of 42mW). An improved address generator is developed in the de-interleavers to reduce the memory bank number of outer deinterleaver from 11 to 1. The embedded memory space requires a total of 158KB allocated as follows: 50KB for FFT, 68KB for equalizer, 1.5KB for Viterbi decoder, 37.8KB for deinterleavers, and 0.7KB for RS decoder.

To reduce power dissipation and avoid invalid signal transition, a multi-stage PM is also integrated into the design. It monitors the working mode of the overall baseband receiver and controls the clock trees and signal transitions. In the initial phase, only the synchronizer and FFT need to work for timing and CFO estimation. Hence, the PM turns off the clock trees and holds the signal transitions from EQ to descrambler. After the acquisition of timing and CFO estimation, the EQ starts to work. Hence, the PM holds the channel estimator and turns on the EQ block and TPS decoder. The TPS decoder decodes the TPS code from EQ output to get sufficient TPS information in one DVB-T/H frame. After successful TPS decoding, the PM turns on the FEC clock tree and only allows signal transitions in data compensation, demodulation, and decoding to reduce power dissipation.

The detailed structure of the OFDM demodulator is shown in Fig. 14.6.2. In the initial phase, the timing synchronizer estimates the Operation Mode (2K/4K/8K), Guard Interval length, and symbol boundary with auto-correlation and power detection. In the meantime, the CFO fraction (<4.6kHz/2.3kHz/1.15kHz for 2K/4K/8K mode) is also estimated from auto-correlation phase. Then the received signal is sent to FFT and the CFO integer is estimated with a monitor of frequency-domain signal drift. The FFT is realized with radix-8 butterfly units, a dynamic wordlength-scaling (DWC) method, and a cache-based architecture to provide 2K/4K/8K modes with less memory power [3]. The DWC dynamically adjusts FFT intra-signal wordlength to achieve minimum memory space for DVB-T/H demodulation. A 64-symbol cache, which temporarily stores the reused signal, is integrated in the FFT to reduce memory access times. After the FFT operation, both time-variant CFR and CFO are estimated and tracked by a 2D linear EQ. The equalized signal is sent to a symbol deinterleaver. In contrast to a traditional approach, symbol interleaving is done before QAM demapping. This is because the 64-level QAM soft-demapping is designed with a 24-bit input and a 36-bit output to achieve the low BER required of DVB-T/H. Therefore interleaving input symbols, rather than output symbols, can reduce memory space by 9KB (12 bits/symbol $\times$ 6048 symbols). After symbol de-interleaving and QAM soft-demapping, the demapped data are sent to the FEC system.

The architecture of time-and-frequency-domain (2D) linear EQ is shown in Fig. 14.6.3. This EQ stores the data of the previous 3 OFDM symbols (S_{-1}, S_{-2}, S_{-3}) and pilots of the previous 4 symbols (S_{-1}, S_{-2}, S_{-3}, S_{-4}) for the 2D CE and correct data compensation. A total 4 time-domain OFDM symbols with 2288 frequency-domain pilots in each OFDM symbol are used to interpolate and track time-variant CFR. Compared with the high-complexity MMSE approach, the proposed CE achieves only a 0.5dB SNR loss for Quasi Error Free (QEF) condition defined by the DVB-T/H system. We also modify the general dual-port SRAM to a pair of single-port SRAM for data storage. Thus data storage area can be reduced by a further 30%.

The detailed FEC design is shown in Fig. 14.6.4. The Viterbi decoder with path merging and path prediction [3] can adaptively adjust the traceback length to reduce power dissipation in the survivor memory. With two dimensional addresses (column and branch address) created by an address generator, the outer deinterleaver is also optimized to utilize the least memory, which is 1128 bytes, only 6 bytes larger than theoretically required. The RS decoder applies the decomposed key equation solver to achieve better area efficiency [4].

Power profiling, chip summary, and the die micrograph of the design implemented in a standard 0.18μm CMOS process is shown in Figs. 14.6.5, 14.6.6, and 14.6.7, respectively. A 109.71MHz system clock is divided to provide the working clocks. Integrating both OFDM demodulator and FEC, the DVB-T/H baseband receiver consumes 250mW power in the highest data rate mode of 31.67Mb/s with 70Hz DF tolerance.

Acknowledgements:
The authors would like to thank UMC for providing shuttle service in this test chip fabrication. They also want to thank CIC for providing testing and measurement facilities.

References:
[1] ETSI EN 300 744 V1.5.1, "Digital Video Broadcasting (DVB): Framing structure, channel coding and modulation for digital terrestrial television," *ETSI*, Nov., 2004.
[2] Yu-Wei Lin, Hsuan-Yu Liu, and Chen-Yi Lee, "A dynamic scaling FFT processor for DVB-T applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 2005-2013, Nov., 2004.
[3] C. C. Lin, Y. H. Shih, H. C. Chang, and C. Y. Lee, "Design of a Power-Reduction Viterbi Decoder for WLAN Applications," *IEEE Trans. Circuits and Systems*, vol. 52, no. 6, pp. 1148-1156, June, 2005.
[4] H.C. Chang, C.B. Shung, and C.Y. Lee, "A Reed–Solomon Product-Code (RS-PC) Decoder Chip for DVD Applications," *IEEE J. Solid-State Circuits*, vol. 1, no. 2, pp. 229-236, Feb., 2001.

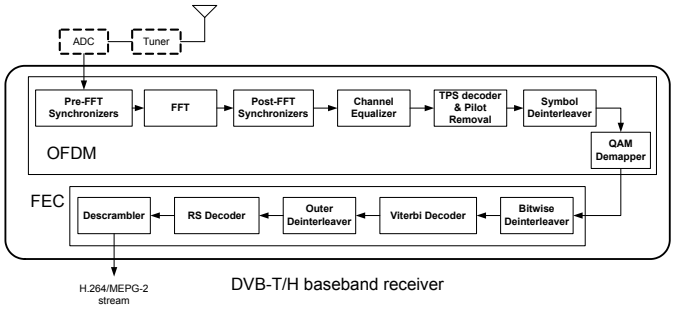

Figure 14.6.1: Block diagram of DVB-T/H baseband receiver.

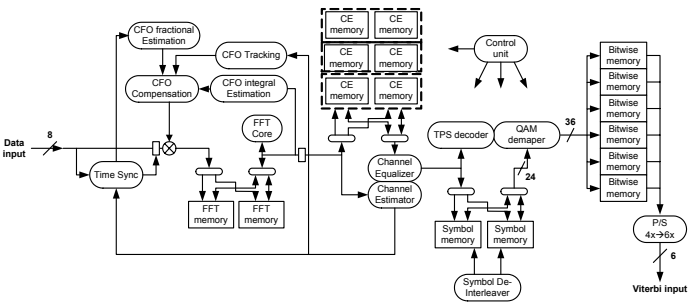

Figure 14.6.2: OFDM architecture for DVB-T/H system.

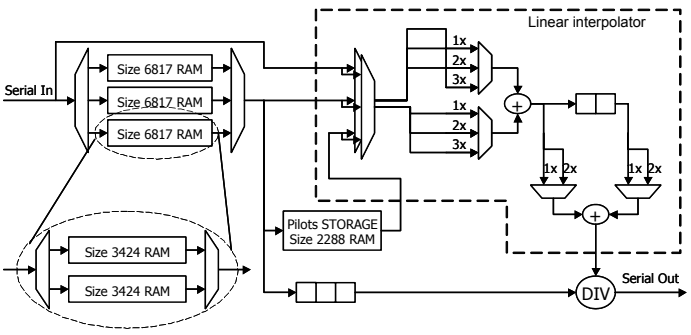

Figure 14.6.3: Architecture of 2D linear channel equalizer.

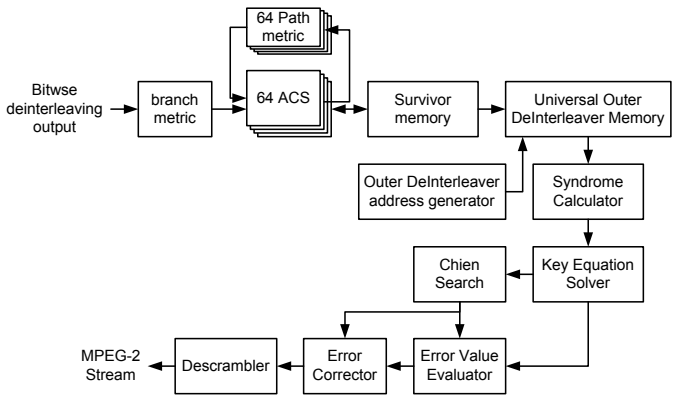

Figure 14.6.4: FEC architecture for DVB-T/H system.

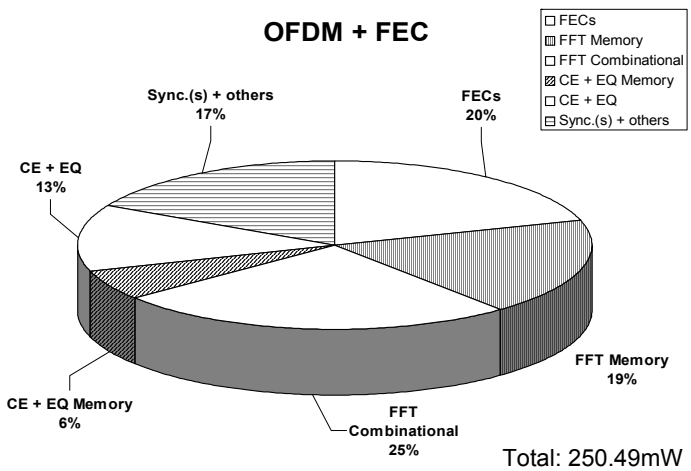

Figure 14.6.5: Power profiling.

Process	**0.18μm CMOS, 1P6M**
Logic Gate Count (Excluding SRAM)	**371K**
Embedded Memory Size	**158 K bytes**
Package	**208-pin CQFP**
Die Size	**6.9 X 5.8 mm²**
Input Clock Speed	**109.71 MHz**
Supply Voltage	**1.8V Core, 3.3V I/O**
Power Consumption	**250mW@31.67Mb/s with 70Hz Doppler freq.**
Supporting Standard	**DVB-T/DVB-H**
Operation mode	**2K, 4K, 8K**
Code Rate	**1/2, 2/3, 3/4, 5/6, 7/8**
Modulation	**QPSK, 16QAM, 64QAM**

Figure 14.6.6: Chip summary.

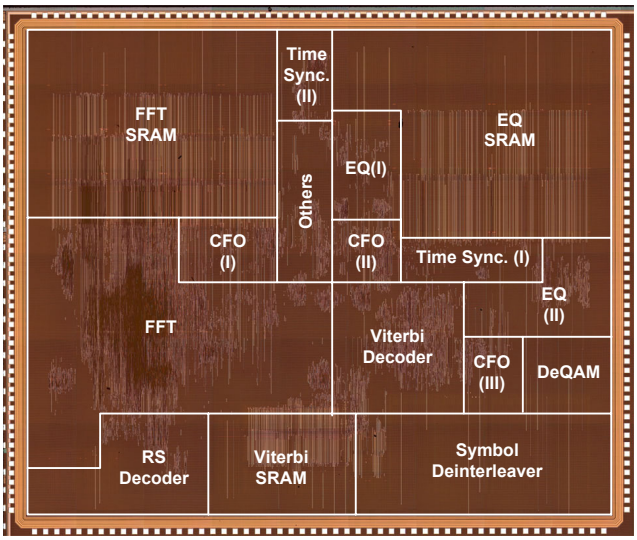

Figure 14.6.7: Chip micrograph.

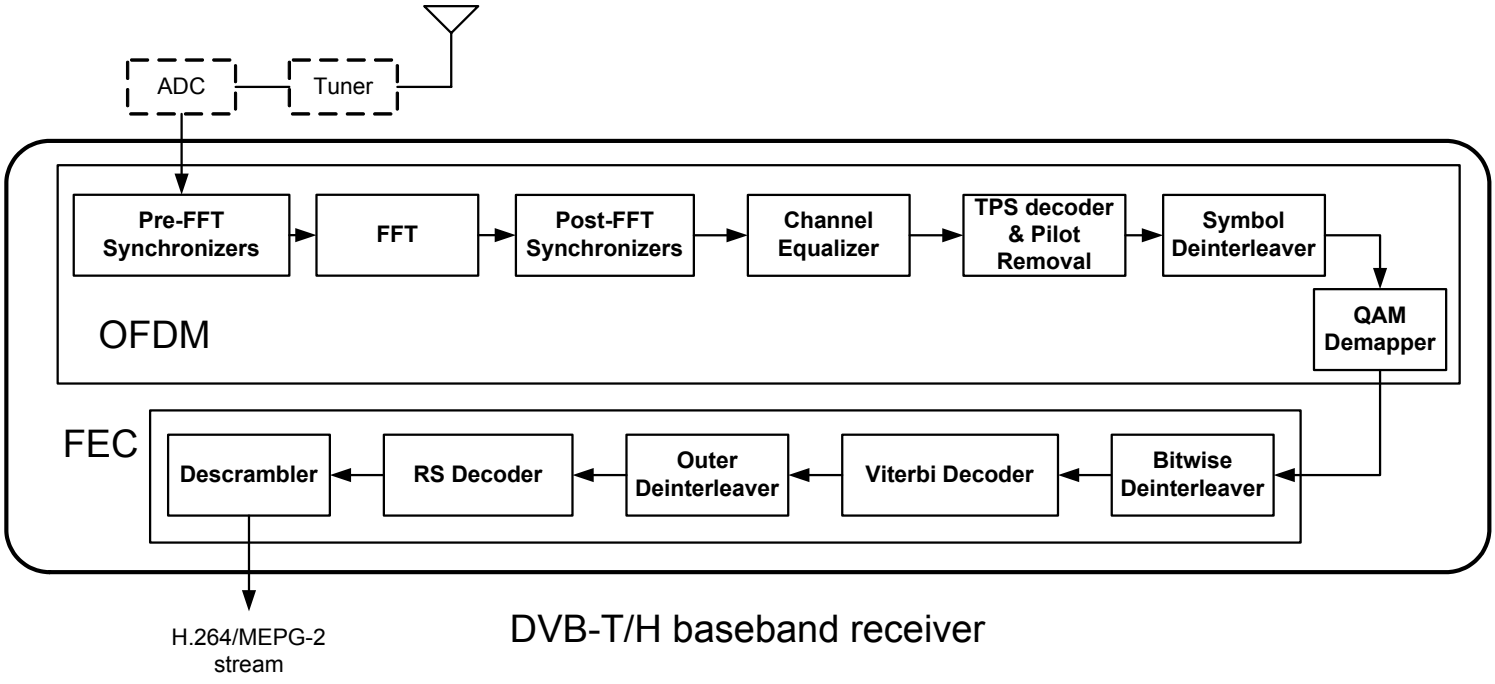

Figure 14.6.1: Block diagram of DVB-T/H baseband receiver.

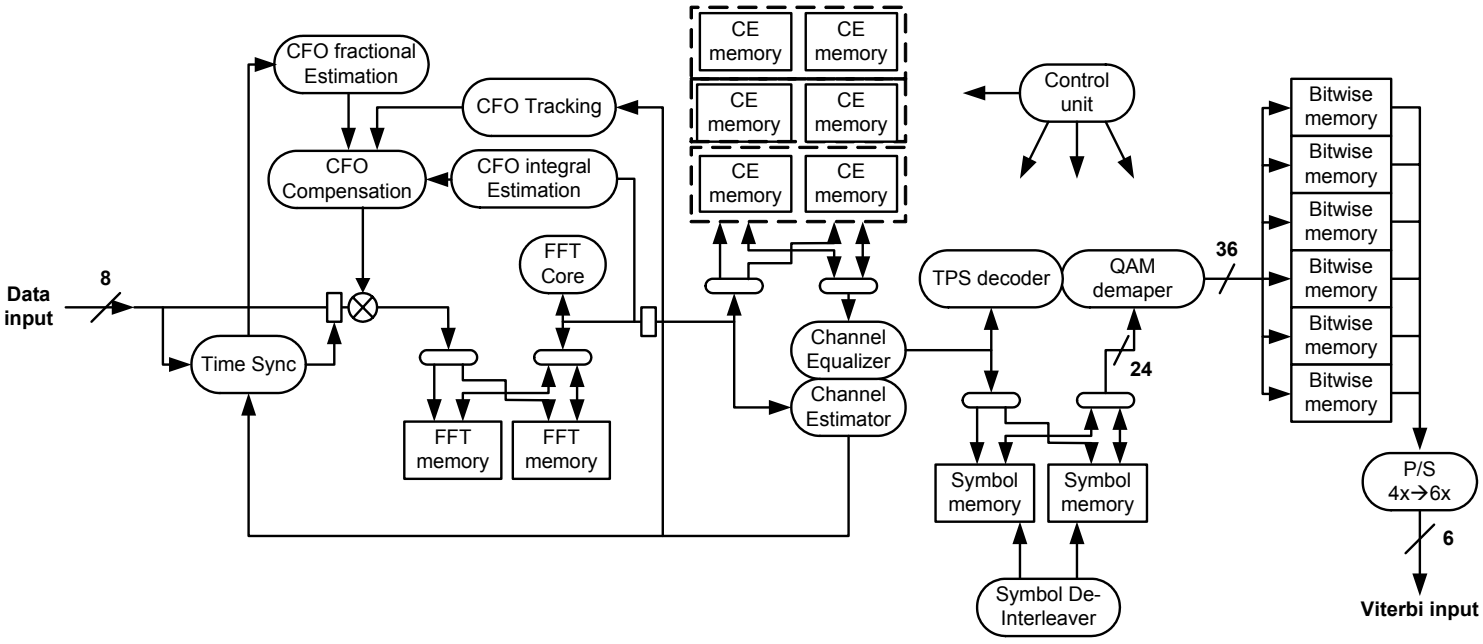

Figure 14.6.2: OFDM architecture for DVB-T/H system.

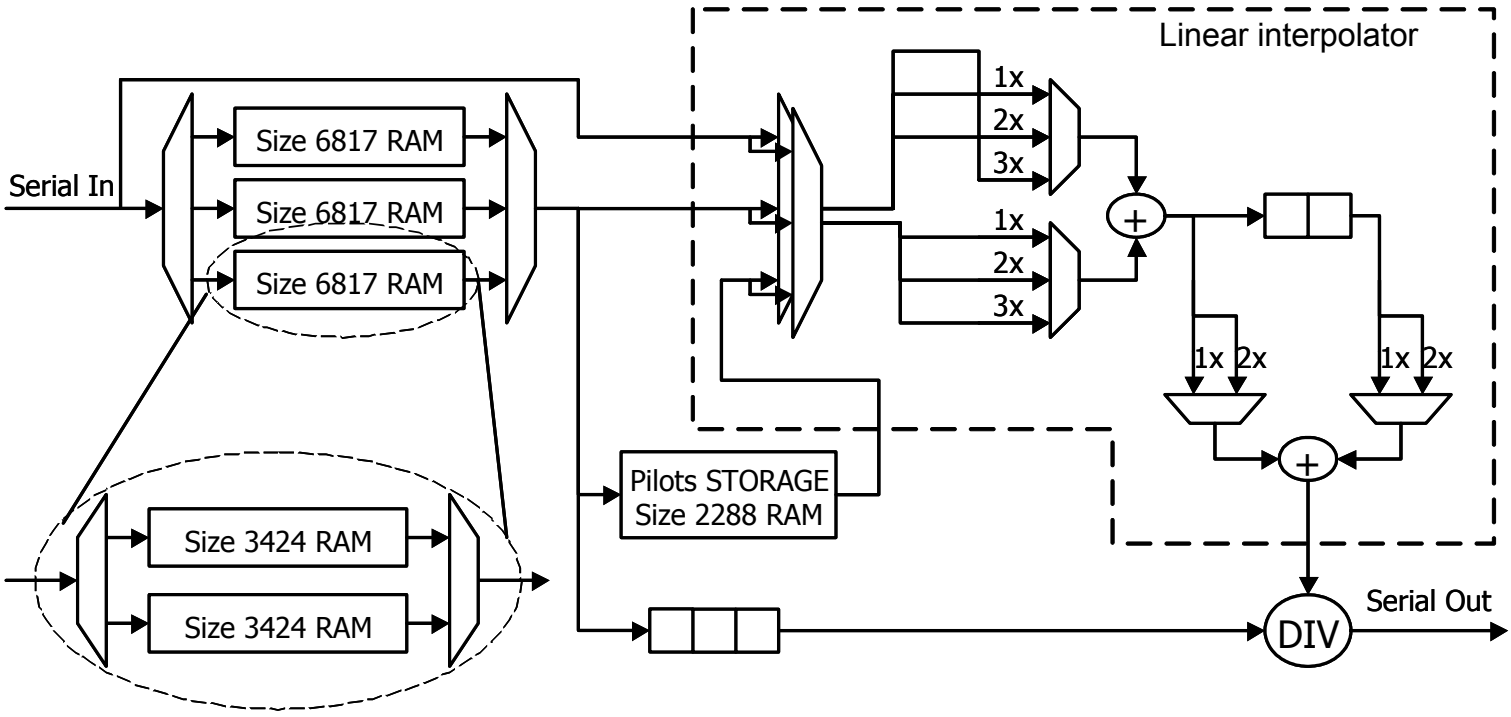

Figure 14.6.3: Architecture of 2D linear channel equalizer.

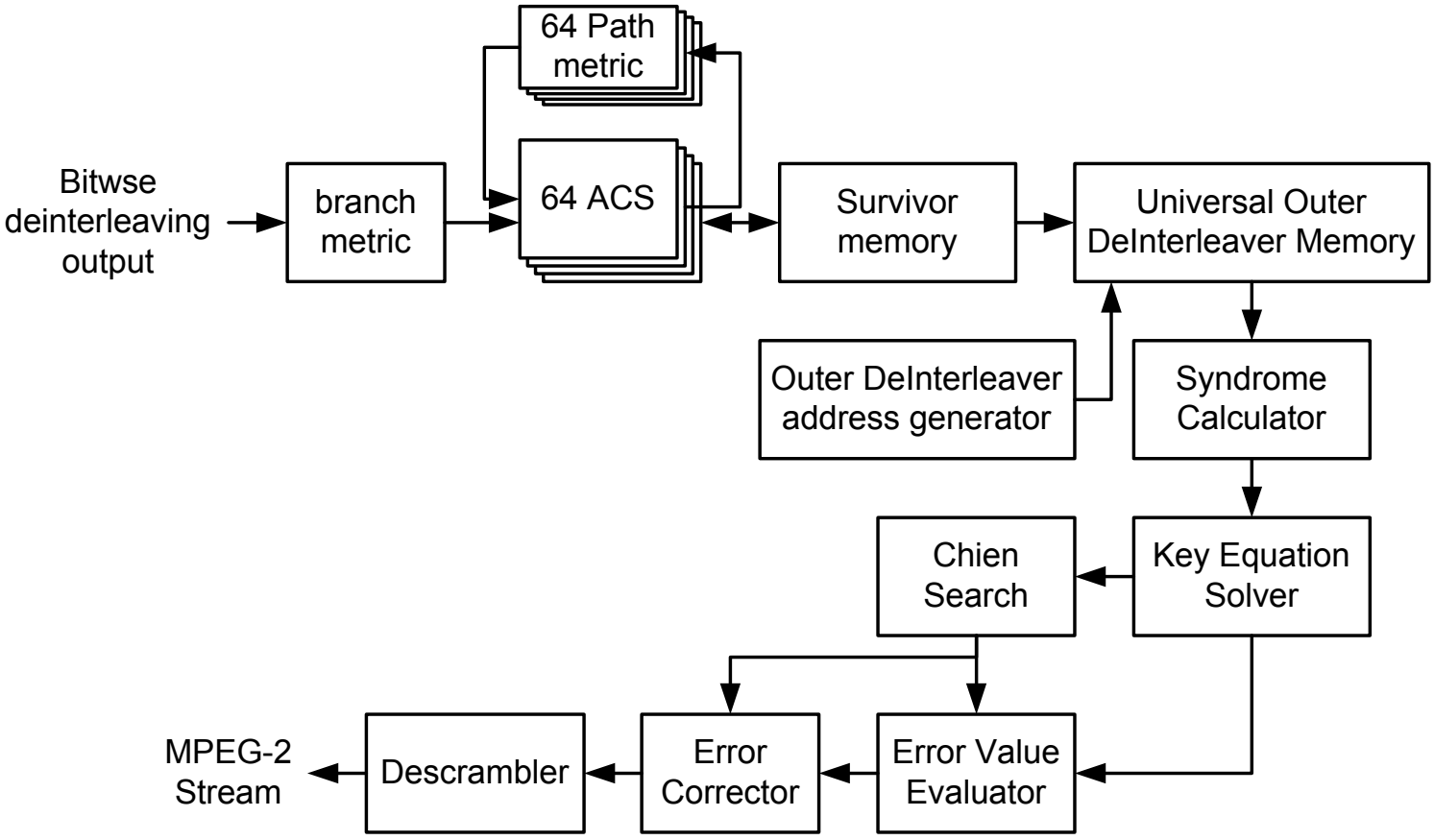

Figure 14.6.4: FEC architecture for DVB-T/H system.

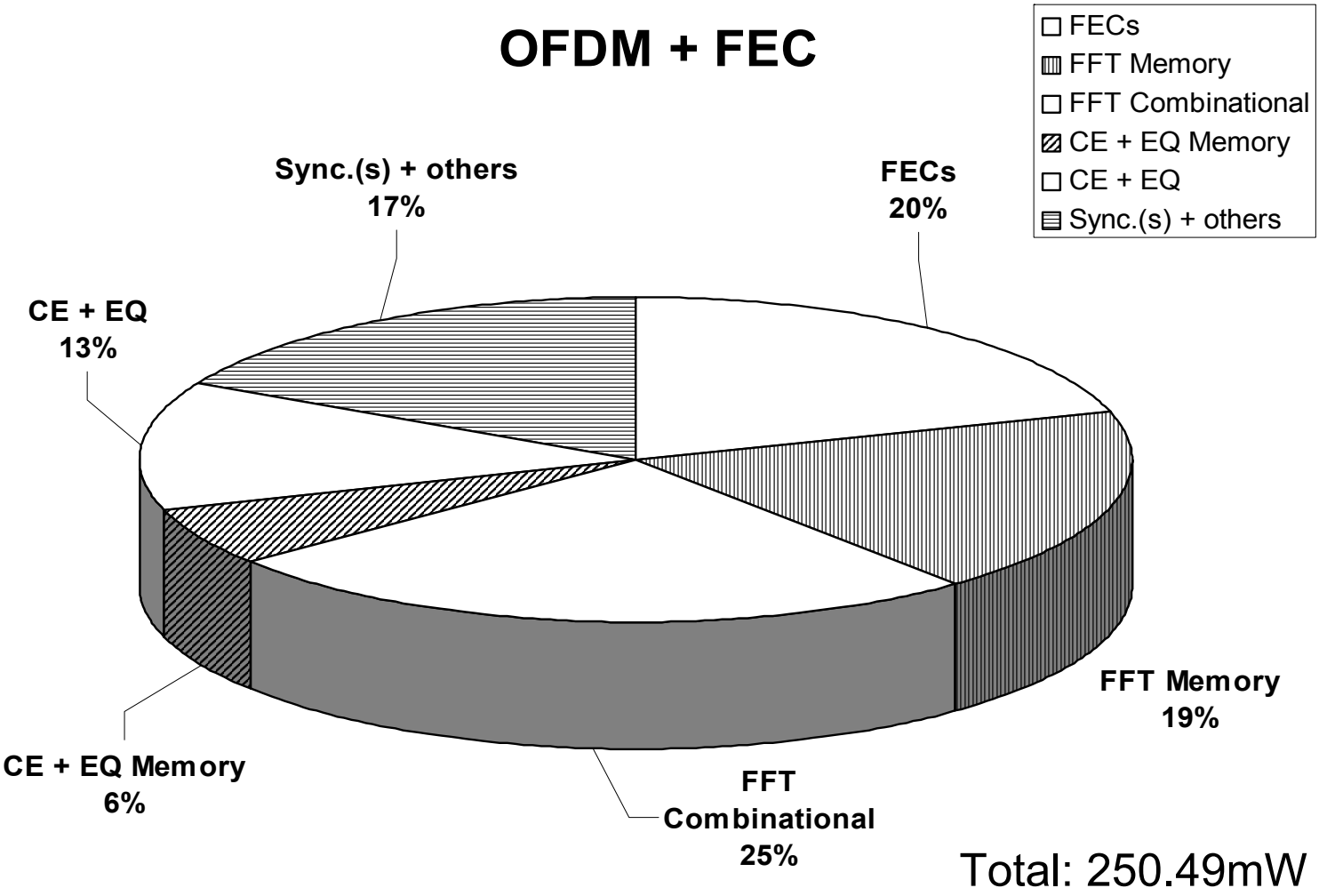

Figure 14.6.5: Power profiling.

Process	**0.18μm CMOS, 1P6M**
Logic Gate Count (Excluding SRAM)	**371K**
Embedded Memory Size	**158 K bytes**
Package	**208-pin CQFP**
Die Size	**6.9 X 5.8 mm^2**
Input Clock Speed	**109.71 MHz**
Supply Voltage	**1.8V Core, 3.3V I/O**
Power Consumption	**250mW@31.67Mb/s with 70Hz Doppler freq.**
Supporting Standard	**DVB-T/DVB-H**
Operation mode	**2K, 4K, 8K**
Code Rate	**1/2, 2/3, 3/4, 5/6, 7/8**
Modulation	**QPSK, 16QAM, 64QAM**

Figure 14.6.6: Chip summary.

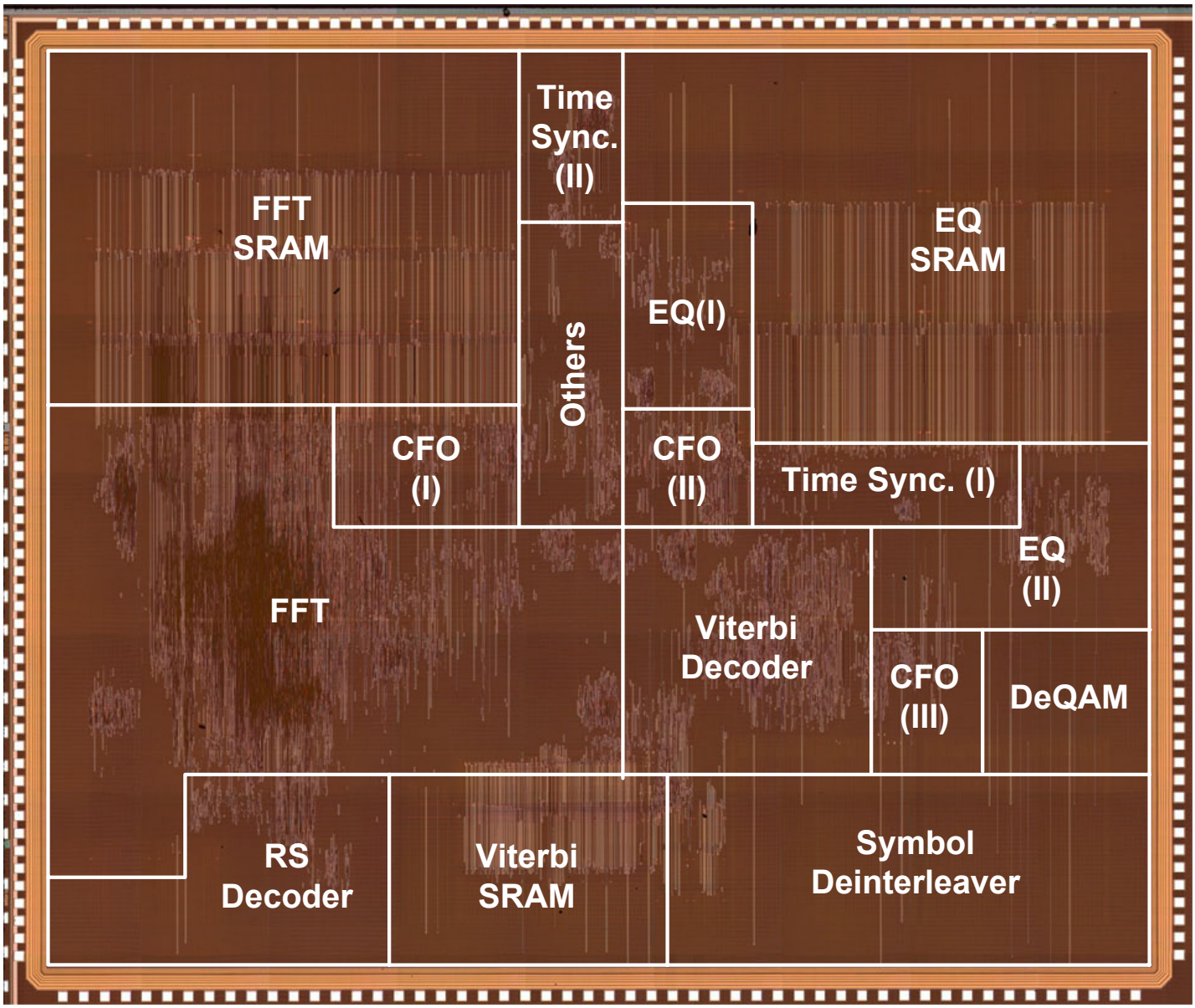

Figure 14.6.7: Chip micrograph.